WHAT IS CLAIMED IS:

1. A power control circuit comprising:
a switch array comprising:
switches;
a flying capacitor; and
an output voltage terminal, capable of providing an output voltage;
a feedback loop, coupled to the output voltage terminal; and
a voltage regulator block, coupled to the feedback loop and to the switch array, the voltage regulator block configured to regulate the output voltage, wherein
at least one of the switches is a segmented switch, comprising more than one switch-segment.

2. The control circuit of Claim 1, wherein
the switch-segments of a segmented switch comprise first and second terminals, wherein
the first terminals of the switch-segments are coupled to a first shared rail; and
the second terminals of the switch-segments are coupled to a second shared rail.

3. The control circuit of Claim 2, wherein
the switch-segments have open and closed switching states, wherein
the conductance between the first and the second shared rail increases when the number of closed switch-segments between the first shared rail and the second shared rail increases.

4. The control circuit of Claim 1, wherein
the switch-segments of a segmented switch are organized into switch-segment groups, wherein
the switch-segment groups can be labeled so that the number of switch-segments in the switch-segment groups are related to each other as increasing powers of two.

5. The control circuit of Claim 1, wherein

the switch-segments comprise transistors, wherein the transistors are selected from the group of bipolar junction transistors and MOS-FETs.

6. The control circuit of Claim 1, wherein:

a first switch is coupled between a first switch node and a second switch node;

a second switch is coupled between the second switch node and a third switch node;

a third switch is coupled between the third switch node and a fourth switch node; and

a fourth switch is coupled between the fourth switch node and a fifth switch node, wherein

the first and third switches are capable of assuming a first switching state, and the second and fourth switches are capable of assuming a second switching state, wherein the first and second switching states are opposite.

7. The control circuit of Claim 6, wherein the flying capacitor is coupled between the second switch node and the fourth switch node.

8. The control circuit of Claim 6, comprising:

an output voltage terminal, coupled to one of the first, third, and fifth switch nodes; and

an output capacitor, coupled to the output voltage terminal.

9. The control circuit of Claim 1, wherein

the voltage regulator block is a digital voltage regulator block.

10. The control circuit of Claim 9, wherein

the digital voltage regulator block is configured to regulate at least one of the switch-segments of at least one segmented switch.

11. The control circuit of Claim 9, the digital voltage regulator block comprising:

an Analog-to-Digital converter; and

an encoder, coupled to the Analog-to-Digital converter, configured to generate a digital error signal from the difference of a reference voltage and a feedback voltage, provided by the feedback loop.

12. The control circuit of Claim 11, the digital voltage regulator block comprising

an add-subtractor, configured to receive the digital error signal from the encoder.

13. The control circuit of Claim 12, wherein

the add-subtractor is configured to receive a sample-and-hold gate signal, and to perform an arithmetic operation on the received digital error signal and the sample-and-hold gate signal.

14. The control circuit of Claim 13, the digital voltage regulator block comprising:

a gate logic, configured:

to receive the signal generated by the add-subtractor;

to generate a gate control signal in accordance with the signal received from the add-subtractor; and

to couple the generated gate control signal into a segmented switch.

15. The control circuit of Claim 14, wherein

the switch-segments have open and closed switching states; and

the number of closed switch-segments is controlled by the received gate control signal.

16. The control circuit of Claim 14, comprising

a link between at least one of the segmented switches and the add-subtractor, the link configured to feed back in an oscillator cycle the gate-signal of the previous oscillator cycle to the add-subtractor, thereby generating a sample-and-hold signal.

17. The control circuit of Claim 1, wherein
the control circuit is configured to operate at a constant frequency.

18. A power control circuit, comprising:
a voltage supply;
a switch array, configured to receive a supply voltage from the voltage supply, comprising:
switches;
at least one capacitor; and
an output voltage terminal;
a feedback loop, coupled to the output voltage terminal; and
a digital voltage regulator block, coupled to the feedback loop, to the voltage supply, and to the switch array, the digital voltage regulator block configured to regulate the supply voltage by digital regulating signals.

19. The control circuit of Claim 18, the switches comprising
segmented switches, wherein
the digital voltage regulator block regulates the segmented switches.

20. A power control circuit, comprising:
a switch array comprising:
switches;
a flying capacitor; and
an output voltage terminal, capable of providing an output voltage;
a feedback loop, coupled to the output voltage terminal; and
a voltage regulator block, coupled to the feedback loop and to the switch array, the voltage regulator block configured to regulate the output voltage, wherein
the power control circuit is operable in charging and pumping phases; and
a ripple of the output voltage is controlled both in the charging and the pumping phase.

21. A power control circuit, comprising:

a voltage supply;

a switch array, configured to receive a supply voltage from the voltage supply, comprising:

switches;

at least one capacitor; and

an output voltage terminal;

a feedback loop, coupled to the output voltage terminal; and

a voltage regulator block, coupled to the feedback loop, to the voltage supply, and to the switch array, the voltage regulator block configured to regulate the supply voltage, wherein

the power control circuit does not include a pass transistor.

22. A method of controlling an output voltage of a power control circuit, the method comprising:

generating an output voltage at an output voltage terminal of the power control circuit;

generating a feedback voltage by feeding the output voltage back to a voltage regulator block by a feedback loop; and

regulating the output voltage according to the feedback voltage by the voltage regulator block controlling at least one segmented switch of a switch array.

23. The method of Claim 22, wherein regulating the output voltage comprises

generating a digital error signal by an Analog-to-Digital converter and a coupled encoder from the difference of a reference voltage and the feedback voltage.

24. The method of Claim 23, wherein regulating the output voltage comprises

generating an add-subtractor signal by performing an arithmetic operation by an add-subtractor on the digital error signal and a sample-and-hold gate signal.

25. The method of Claim 24, wherein regulating the output voltage comprises:

generating a gate control signal by a gate logic in accordance with the add-subtractor signal; and

coupling the gate control signal into the switch array.

26. The method of Claim 25, wherein regulating the output voltage comprises

controlling the number of closed switch-segments of the switch array by the gate control signal, wherein

the switch-segments have open and closed switching states.

27. A method of controlling an output voltage of a power control circuit, the method comprising:

providing a supply voltage by a voltage supply to a switch array;

generating an output voltage at an output voltage terminal;

generating a feedback voltage by feeding the output voltage back to a digital voltage regulator block by a feedback loop; and

regulating the output voltage by the digital voltage regulator block digitally controlling at least one switch of the switch array according to the feedback voltage.

28. The method of Claim 27, wherein at least one of the switches comprises at least one segmented switch.

29. A method of controlling an output voltage of a power control circuit, the method comprising:

providing a power control circuit, comprising:

a switch array comprising:

switches;

a flying capacitor; and

an output voltage terminal, capable of providing an output voltage;

a feedback loop, coupled to the output voltage terminal; and

a voltage regulator block, coupled to the feedback loop and to the switch array, the voltage regulator block configured to regulate the output voltage;

operating the power control circuit in charging and pumping phases; and

controlling a ripple of the output voltage both in the charging and the pumping phase.